124 has p type conductivity. Contact region 124 is formed on a portion of p type body layer 122 so as to be connected to p type body layer 122.

Further, referring to FIG. 2 and FIG. 3, epitaxial substrate 100 has a trench TR provided with an inner surface having side wall surfaces SW and a bottom surface BT. Each of side wall surfaces SW extends through n region 123 and p type body layer 122 and reaches n^- layer 121. Bottom surface BT is formed of n^- layer 121. Side wall surface SW has a channel surface CH (FIG. 3) on p type body layer 122. Preferably, side wall surface SW has a predetermined crystal plane (also referred to as "special plane") particularly on p type body layer 122. Details of the special plane will be described later.

The fact that epitaxial substrate 100 has trench TR corresponds to such a fact that the epitaxial layer is partially removed above the upper surface of single-crystal substrate 110. In the present embodiment, a multiplicity of mesa structures are formed on the upper surface of single-crystal substrate 110. Specifically, each of the mesa structures has an upper surface and a bottom surface both having a hexagonal shape, and has side walls inclined relative to the upper surface of single-crystal substrate 110. Thus, trench TR expands in a tapered shape toward the opening.

Gate oxide film 201 (FIG. 1) covers the inner surface of trench TR, namely, side wall surfaces SW and bottom surface BT. Gate oxide film 201 has a thickness TA (FIG. 4) on side wall surface SW formed of p type body layer 122. Gate oxide film 201 also has a thickness TB (FIG. 4) on bottom surface BT. Thickness TB is larger than thickness TA. Preferably, thickness TB is larger than thickness TA by 300 nm or more.

Gate oxide film 201 includes a first portion 201A formed by thermal oxidation of silicon carbide, and a second portion 201B formed by thermal oxidation of silicon. At least a portion of second portion 201B is provided on bottom surface BT of trench TR with first portion 201A interposed therebetween.

Second portion 201B has a carbon atom concentration lower than that of first portion 201A. First portion 201A may have a carbon atom concentration of more than 1×10^{15} cm^{-3}. Second portion 201B preferably has a carbon atom concentration of less than 1×10^{15} cm^{-3}. It should be noted that in the case where the carbon atom concentrations are not uniform, an average value may be calculated.

A portion where bottom surface BT and side wall surface SW of trench TR are connected to each other forms a corner portion RS (FIG. 5). First portion 201A provided on corner portion RS forms a corner portion RA having a radius of curvature approximately similar to that of corner portion RS. Second portion 201B provided on corner portion RA forms a corner portion RB having a radius of curvature greater than that of corner portion RA. Thus, an electric field is relaxed in corner portion RB.

Gate electrode 202 is buried in trench TR with gate oxide film 201 interposed therebetween. Gate oxide film 201 separates epitaxial substrate 100 and gate electrode 202 from each other in trench TR. Gate electrode 202 faces the surface of p type body layer 122 with gate oxide film 201 interposed therebetween. Gate electrode 202 has an upper surface substantially as high as the upper surface of a portion of gate oxide film 201 on the upper surface of n region 123. Interlayer insulating film 203 is provided to cover gate electrode 202 as well as the extended portion of gate oxide film 201 on the upper surface of n region 123.

Source electrode 221 extends through interlayer insulating film 203 and makes contact with each of n region 123 and contact region 124. Source interconnection 222 is provided on source electrode 221 and interlayer insulating film 203 in contact with source electrode 221. Drain electrode 211 is provided on an opposite surface of epitaxial substrate 100 to its surface in which trench TR is provided. Protecting electrode 212 covers drain electrode 211.

A method for manufacturing MOSFET 500 (FIG. 1) is now described.

As shown in FIG. 6, on single-crystal substrate 110, n^- layer 121 is formed by means of epitaxial growth. This epitaxial growth can be performed by means of, for example, a CVD (Chemical Vapor Deposition) method in which a mixed gas of silane (SiH_4) and propane (C_3H_8) is used as a source material gas and hydrogen gas (H_2) is used as a carrier gas, for example. In doing so, it is preferable to introduce nitrogen (N) or phosphorus (P) as a donor, for example.

As shown in FIG. 7, p type body layer 122 is formed on n^- layer 121, and n region 123 is formed on p type body layer 122. Specifically, ion implantation is performed into the upper surface of n^- layer 121. In the ion implantation for forming p type body layer 122, ions of an acceptor such as aluminum (Al) are implanted. Meanwhile, in the ion implantation for forming n region 123, ions of a donor such as phosphorus (P) are implanted. Thus, epitaxial substrate 100 is formed which has n^- layer 121, p type body layer 122, and n region 123. It should be noted that instead of the ion implantation, epitaxial growth involving addition of impurities may be employed.

As shown in FIG. 8, contact regions 124 are formed by ion implantation. Next, activation heat treatment is performed to activate the impurities added by the ion implantation. This heat treatment is preferably performed at a temperature of not less than 1500° C. and not more than 1900° C., for example, a temperature of approximately 1700° C. The heat treatment is performed for approximately 30 minutes, for example. The atmosphere of the heat treatment is preferably an inert gas atmosphere, such as Ar atmosphere.

Next, a mask 247 (FIG. 9) having an opening through which n region 123 is partially exposed is formed on epitaxial substrate 100. The opening is formed to correspond to the location of trench TR (FIG. 1). As mask 247, a silicon oxide film formed by thermal oxidation can be used, for example.

As shown in FIG. 10, in the opening of mask 247, n region 123, p type body layer 122, and a portion of n^- layer 121 are removed by etching. An exemplary, usable etching method is reactive ion etching (RIE), in particular, inductively coupled plasma (ICP) RIE. Specifically, ICP-RIE can be employed in which SF_6 or a mixed gas of SF_6 and O_2 is used as the reactive gas, for example. By means of such etching, in the region where trench TR (FIG. 1) is to be formed, a recess TQ can be formed which has a side wall having an inner surface SV substantially perpendicular to the main surface of single-crystal substrate 110.

Next, epitaxial substrate 100 is etched using mask 247. Specifically, inner surface SV of recess TQ of epitaxial substrate 100 is thermally etched. The thermal etching can be performed, for example, by heating epitaxial substrate 100 in an atmosphere including a reactive gas containing at least one or more types of halogen atom. The at least one or more types of halogen atom include at least one of chlorine (Cl) atom and fluorine (F) atom. This atmosphere is, for example, Cl_2, BCL_3, SF_6, or CF_4. For example, the thermal etching is performed using a mixed gas of chlorine gas and